CLAIMS:

1. A method for reducing line-to-line capacitance, comprising:

forming a low dielectric constant (K) material over a semiconductor substrate;

forming a standard K material over the low-K material;

forming a conductive material proximate the low-K material and the standard K material; and

forming a barrier layer disposed between the low-K material and the conductive material before forming the conductive material.

2. The method of Claim 1 wherein forming the low-K material comprises forming the low-K material from a material selected from the group consisting of a hydrogen silsesquioxane, a methyl silsesquioxane, a polyarylene ether, a fluorine-comprising silicon oxide and a carbon-comprising silicon oxide.

3. The method of Claim 1 wherein forming the low-K material comprises forming the low-K material from a spin-on low-K precursor material.

4. The method of Claim 1 wherein forming the low-K material comprises forming the low-K material employing a chemical vapor deposition process.

5. The method of Claim 1 wherein forming the standard K material comprises forming a layer of a silicon oxide material.

6. The method of Claim 5 wherein forming the layer of silicon oxide material comprises forming the silicon oxide material employing a chemical vapor deposition process.

7. The method of Claim 1 wherein forming the conductive material proximate the low-K material and the standard K material comprises forming the conductive material from a copper-comprising material.

8. The method of Claim 1 wherein forming the conductive material proximate the low-K material and the standard K material comprises forming the conductive material from an aluminum-comprising material.

9. The method of Claim 1 wherein forming the barrier layer comprises forming a diffusion barrier comprising nitrogen.

10. The method of Claim 9 wherein forming the diffusion barrier comprising nitrogen comprises forming the diffusion barrier of a material selected from the group consisting of a silicon nitride material, a silicon oxynitride material, a refractory metal nitride material, a hydrogen and nitrogen-comprising amorphous carbon material and a silicon and nitrogen-comprising amorphous carbon material.

11. The method of Claim 1 wherein forming the conductive material proximate the low-K material and the standard K material comprises etching the low-K material and the standard K material to form a recess and forming the conductive material such that the recess is essentially completely filled with the conductive material.

12. The method of Claim 11 wherein etching the low-K material and the standard K material comprises etching to form a plurality of recesses such that the plurality of recesses define a plurality of spaced apart dielectric-comprising blocks are formed, and forming the conductive material comprises forming such that each of the plurality of recesses is essentially filled with the conductive material such that a plurality of interconnects is formed, each interconnect separated from another by a spaced apart dielectric block.

13. The method of Claim 1, further comprising:

patterning the low-K material and the standard K material to form spaced blocks over the substrate;

forming a conductive material over and between the spaced blocks;

planarizing the conductive material to expose the standard K material of the spaced blocks and to form an array of conductive interconnects between the spaced blocks;

removing the exposed standard K material from over the low-K material of the spaced blocks; and

forming a second layer of low-K material over the conductive material and the low-K material of the spaced blocks.

14. The method of Claim 13 further comprising forming a conformal barrier layer over the spaced blocks before forming the conductive material over and between the spaced blocks such that after forming the conductive material a portion of the conformal barrier layer is disposed between the spaced blocks and the conductive material.

15. The method of Claim 14 further comprising removing portions of the conformal barrier layer overlying an upper surface of the standard K material prior to forming the conductive material.

16. A semiconductive processing method, comprising:

forming a low dielectric constant (K) material over a semiconductor substrate;

forming a sacrificial material over the low-K material, the sacrificial material not being a low-K material;

forming a conductive material over and adjacent the sacrificial material; and

removing the conductive material and sacrificial material from over the low-K material.

17. The method of Claim 16 wherein forming the low-K material comprises forming the low-K material from a liquidus low-K precursor material.

18. The method of Claim 16 wherein removing the conductive material comprises removing the material employing a chemical mechanical polishing process.

19. The method of Claim 16 wherein removing the sacrificial material comprises removing the material employing a plasma etching process.

20. The method of Claim 16 further comprising forming a second low-K material over the low-K material disposed over the substrate and the metal layer, after removing the sacrificial material.

21. The method of Claim 20 wherein forming the second low-K material comprises forming the second material from a material selected from the group consisting of a hydrogen silsesquioxane, a methyl silsesquioxane, a polyarylene ether, a fluorine-comprising silicon oxide and a carbon-comprising silicon oxide after forming a conformal barrier layer over the metal layer, the conformal barrier layer selected form the group consisting of a silicon nitride material, a silicon oxynitride material, a refractory metal nitride material, a hydrogen and nitrogen-comprising amorphous carbon material and a silicon and nitrogen-comprising amorphous carbon material.

22. A semiconductor processing method, comprising:

forming a low-K dielectric material over a substrate;

forming a second material over the low-K dielectric material;

patterning the low-K dielectric material and second material to form spaced apart blocks over the substrate; and

forming a conductive material over and between the spaced apart blocks.

23. The method of Claim 22 further comprising forming a conformal barrier layer over the spaced apart blocks prior to forming the conductive material.

24. The method of Claim 23 further comprising removing the conductive material from over the spaced apart blocks to form a plurality of conductive interconnects.

25. The method of Claim 24 wherein removing the conductive material comprises removing the material employing a chemical mechanical polishing process.

26. The method of Claim 23 wherein forming the conductive material comprises forming a copper comprising material or an aluminum comprising material.

27. A semiconductor structure, comprising:

a semiconductive material substrate;

a plurality of spaced blocks over the semiconductive substrate, the blocks comprising a lower portion comprising a low dielectric constant (K) material and an upper portion having a different insulative composition than the lower portion, the upper portion defining a substantially planar upper surface of the block; and

a conductive material disposed between the spaced blocks, the conductive material having an upper surface substantially planar and coextensive with the upper surface of the block.

28. The structure of Claim 27 further comprising a barrier material disposed between the conductive material and the spaced blocks, the barrier layer having a first surface in contact with the lower portion, the upper portion and an opposing second surface in contact with the conductive material.

29. The structure of Claim 28 further comprising:

a second barrier layer disposed over the upper surface of the spaced blocks and the conductive material; and

a layer of dielectric material disposed over the second barrier layer, the dielectric material comprising a low-K material and having an essentially planar upper surface.

30. The structure of Claim 29 further comprising:

a plurality of contact openings disposed within the layer of dielectric material, each contact opening extending from the upper surface of the layer of dielectric material through the second barrier layer to a portion of the upper surface of the conductive material; and

a second conductive material disposed within and essentially filling the contact openings.